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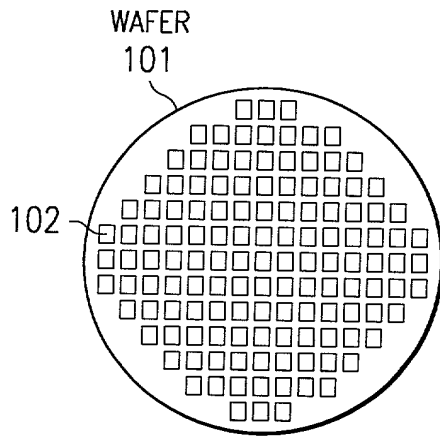


FIG. 1A

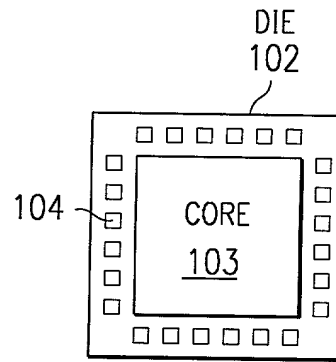


FIG. 1B

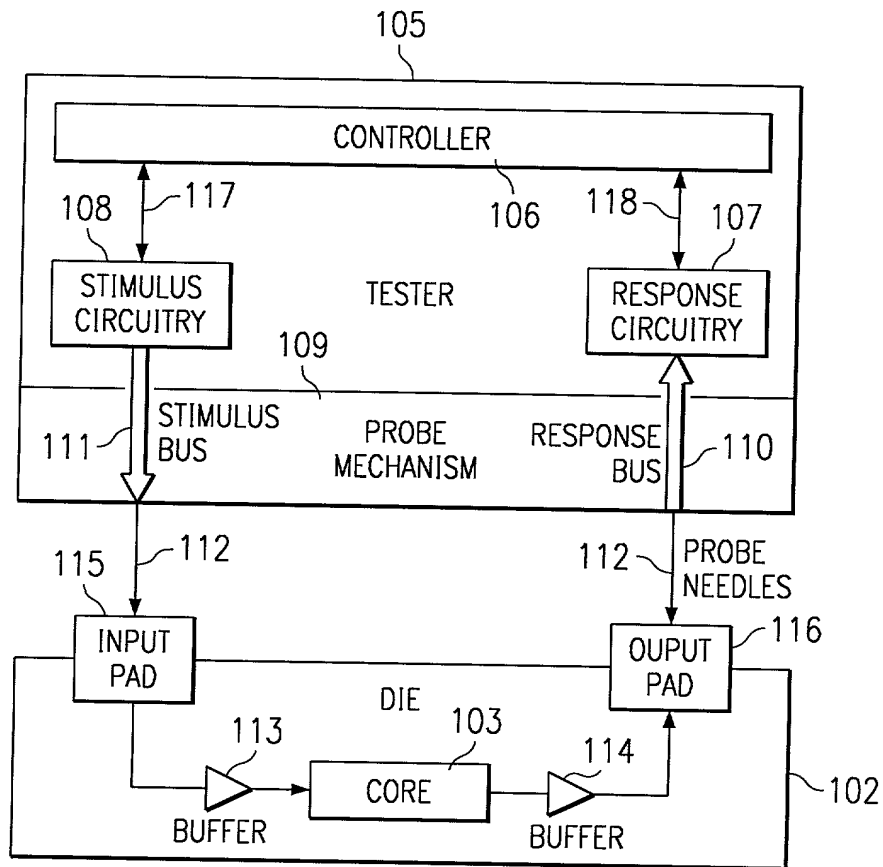


FIG. 1C

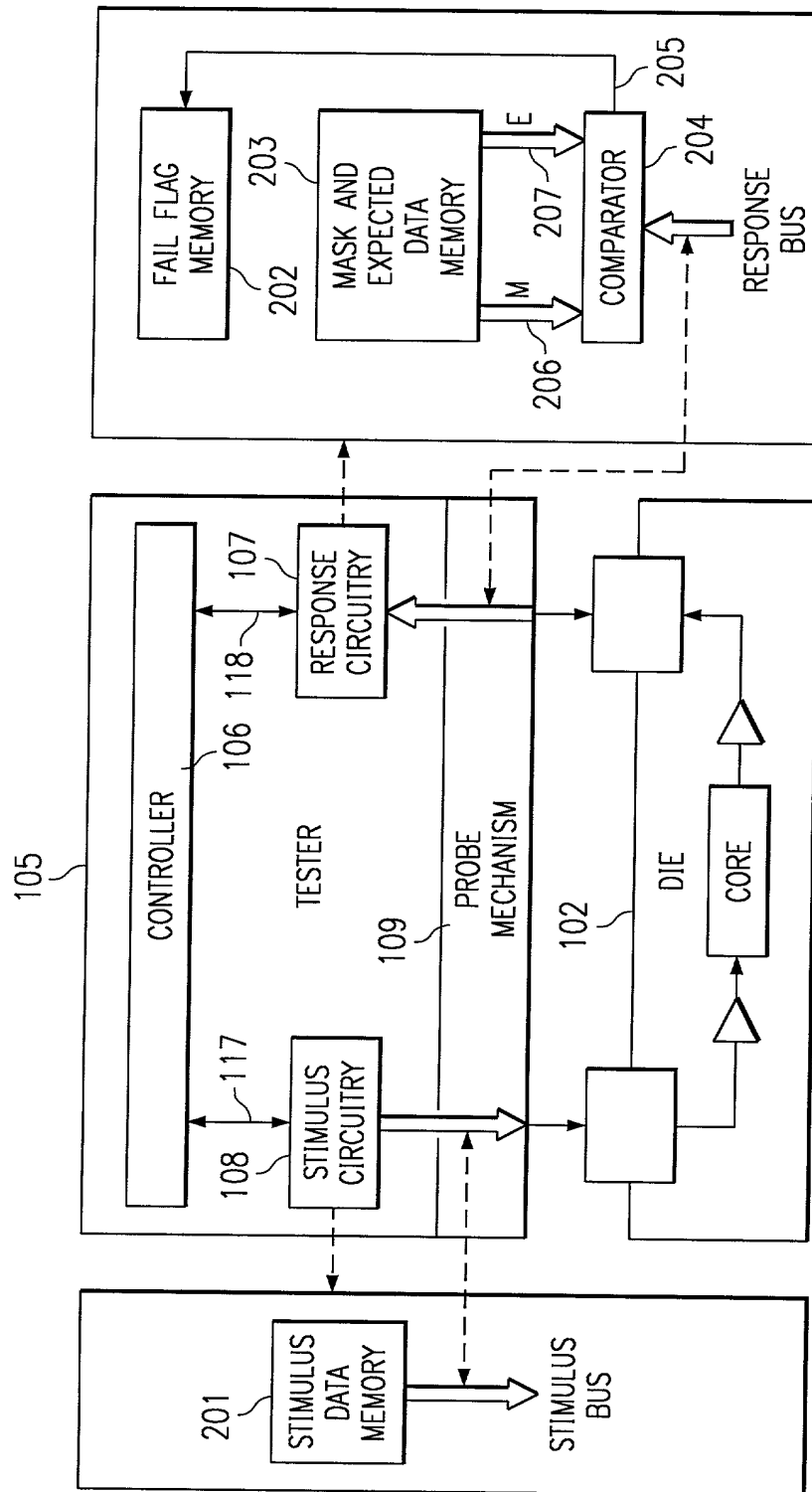


FIG. 2

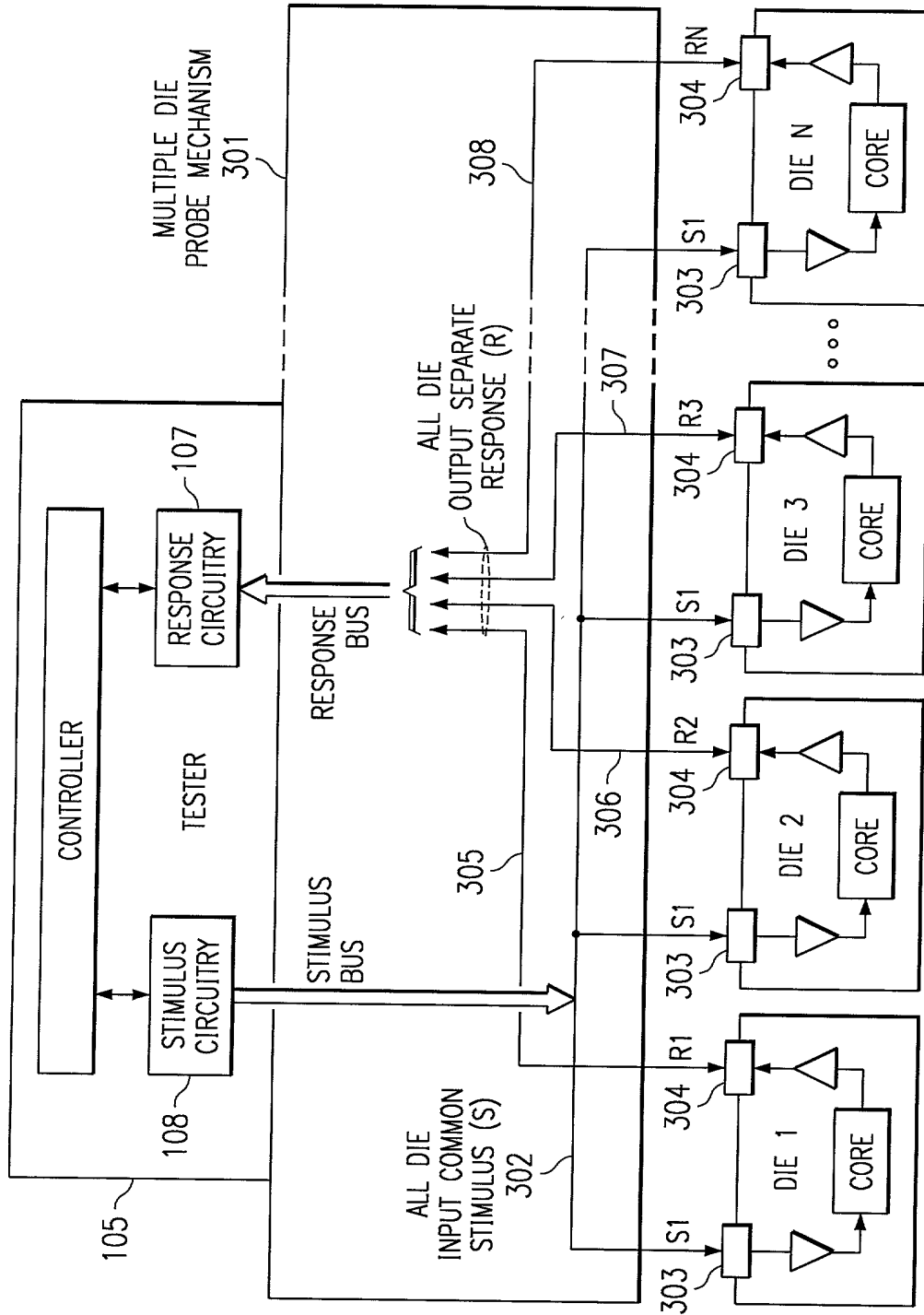


FIG. 3

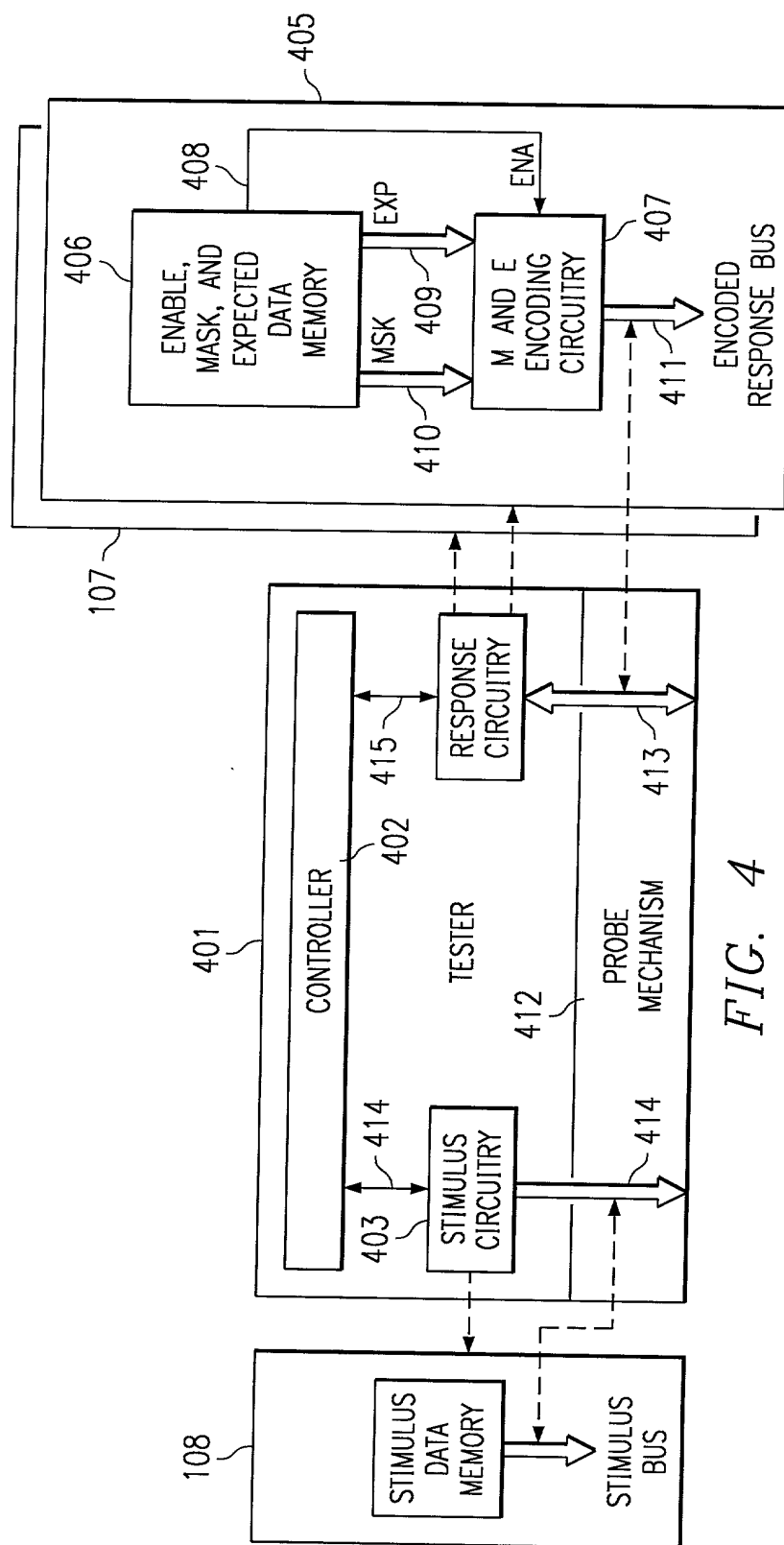


FIG. 4

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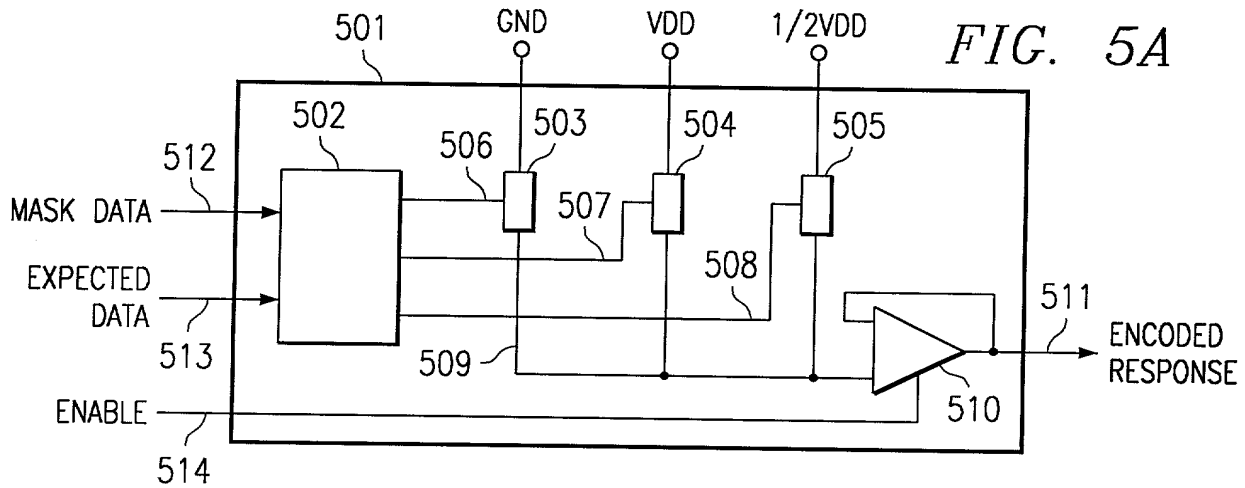
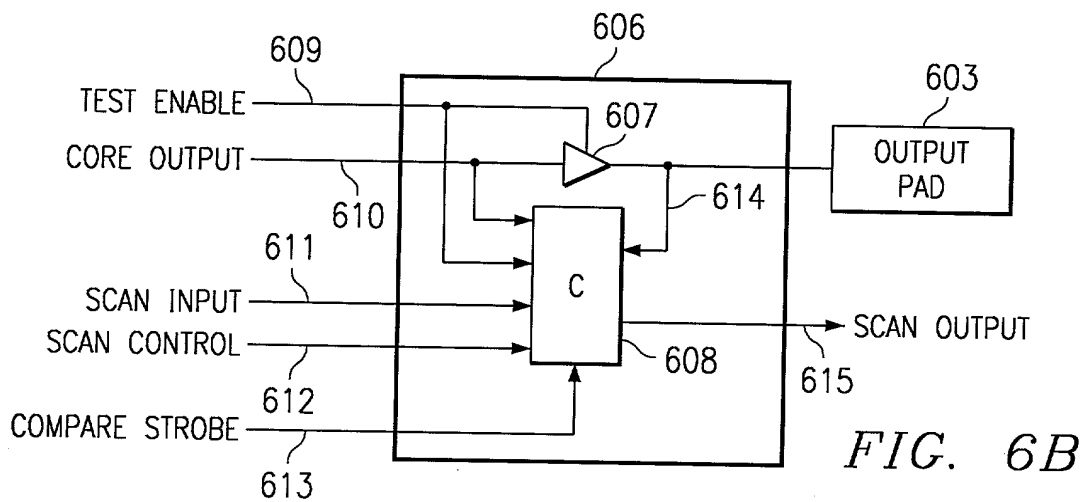
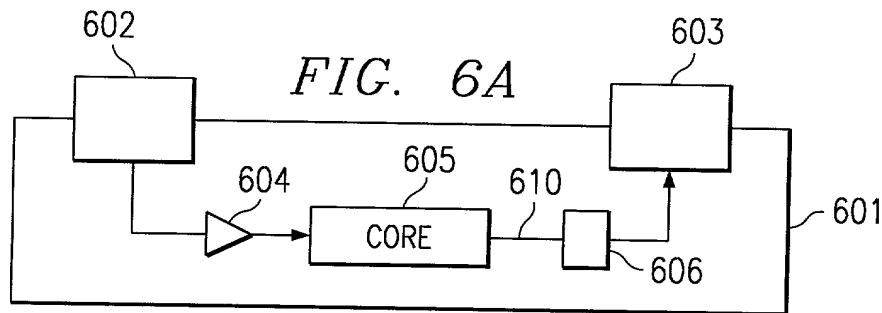


FIG. 5B

ENA	MSK	EXP	ENR	OUTPUT MODE
0	0	0	Z	DISABLED
1	0	0	GND	LOW
1	0	1	VDD	HIGH
1	1	X	1/2VDD	MASK



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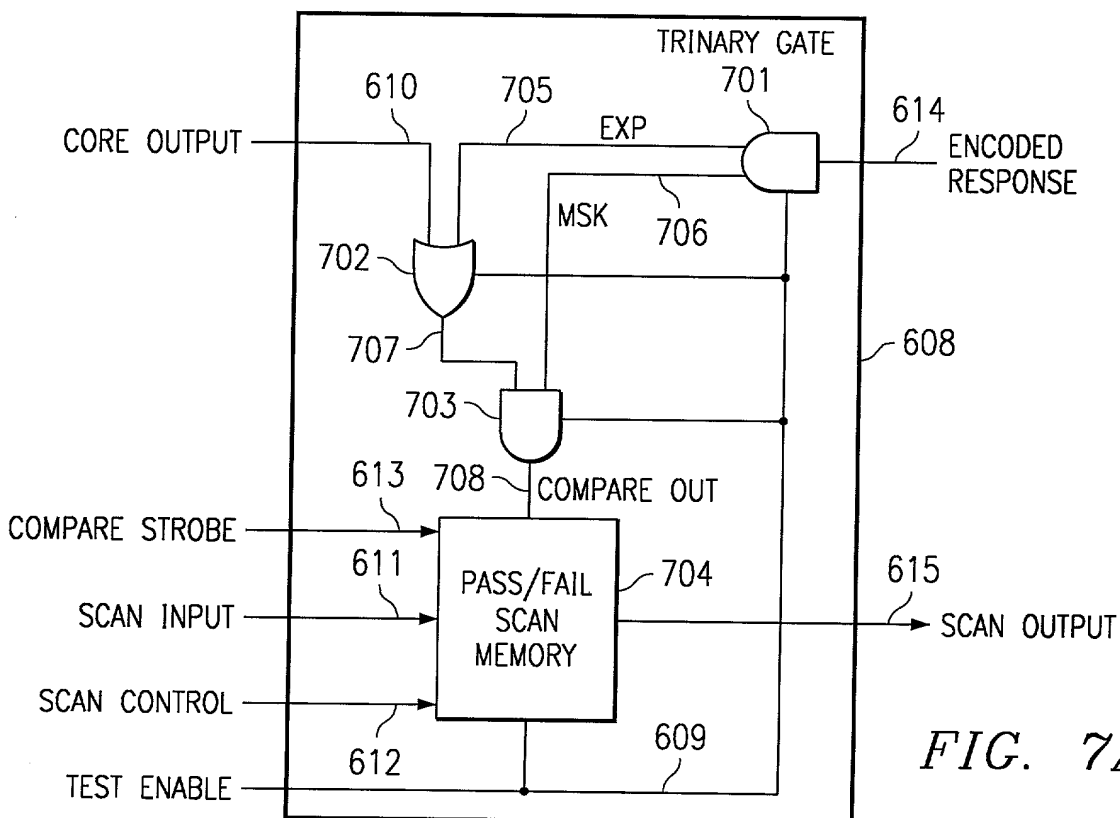


FIG. 7A

TEN	ENR	MSK	EXP	FUNCTION PERFORMED
0	X	X	X	TEST DISABLED
1	GND	1	0	COMPARE LOW
1	VDD	1	1	COMPARE HIGH
1	1/2VDD	0	X	MASK COMPARE

FIG. 7B

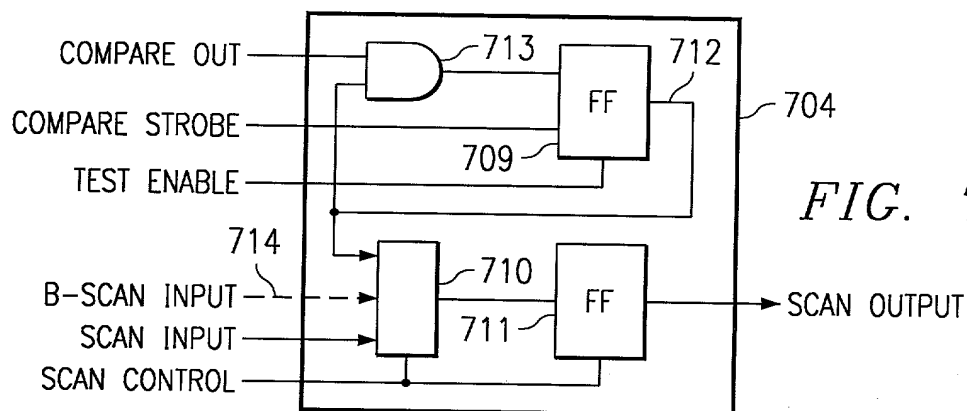


FIG. 7C

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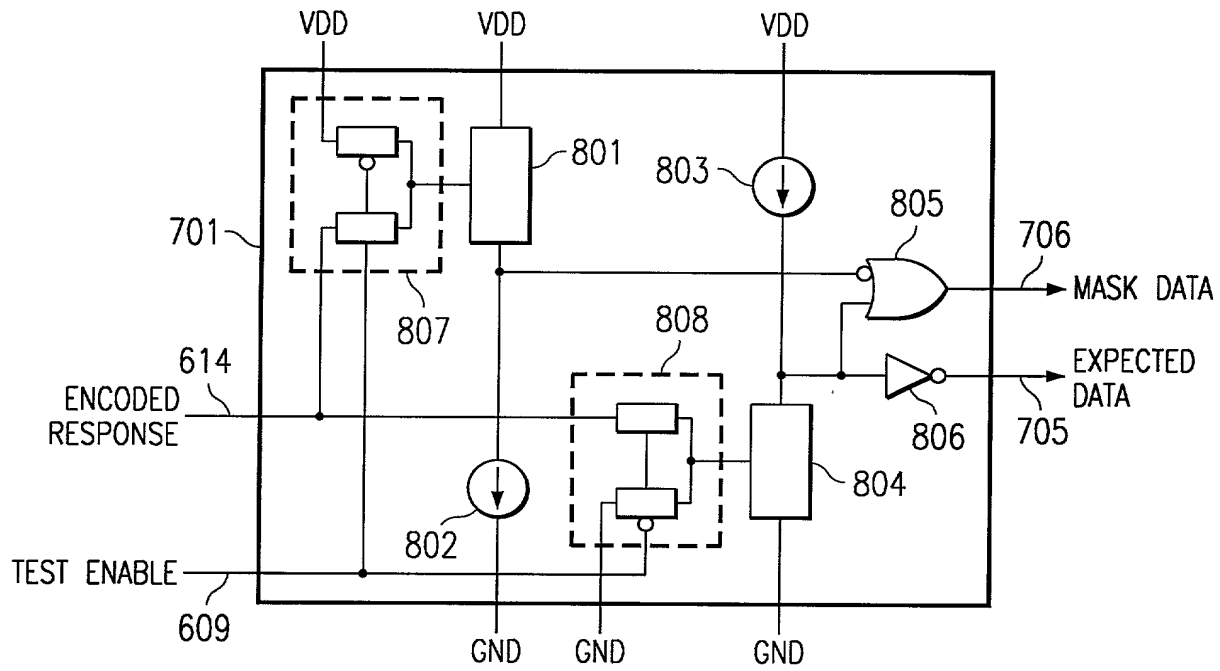


FIG. 8A

TEN	ENR	MSK	EXP	FUNCTION PERFORMED
0	X	1	0	GATE DISABLED
1	GND	1	0	OUTPUT A LOW
1	VDD	1	1	OUTPUT A HIGH
1	1/2VDD	0	X	OUTPUT A MASK

FIG. 8B

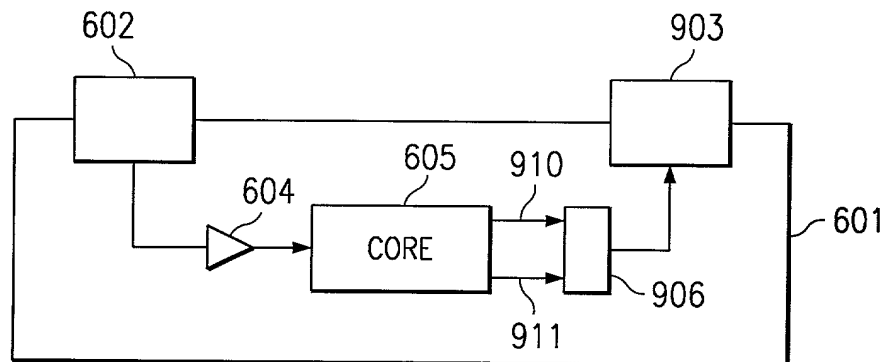


FIG. 9A

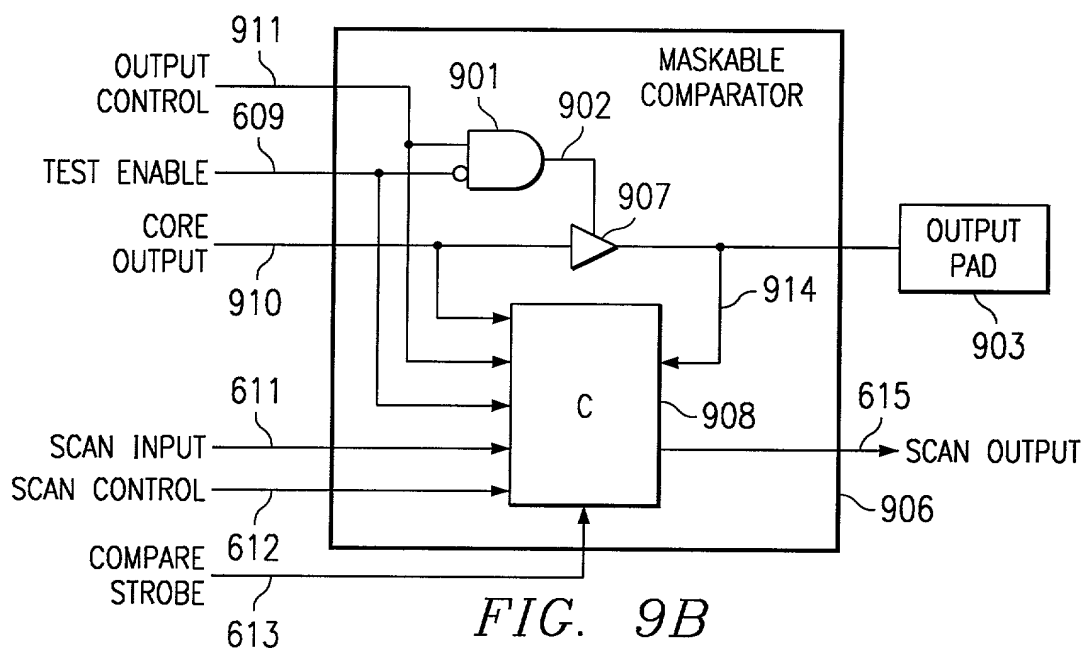


FIG. 9B

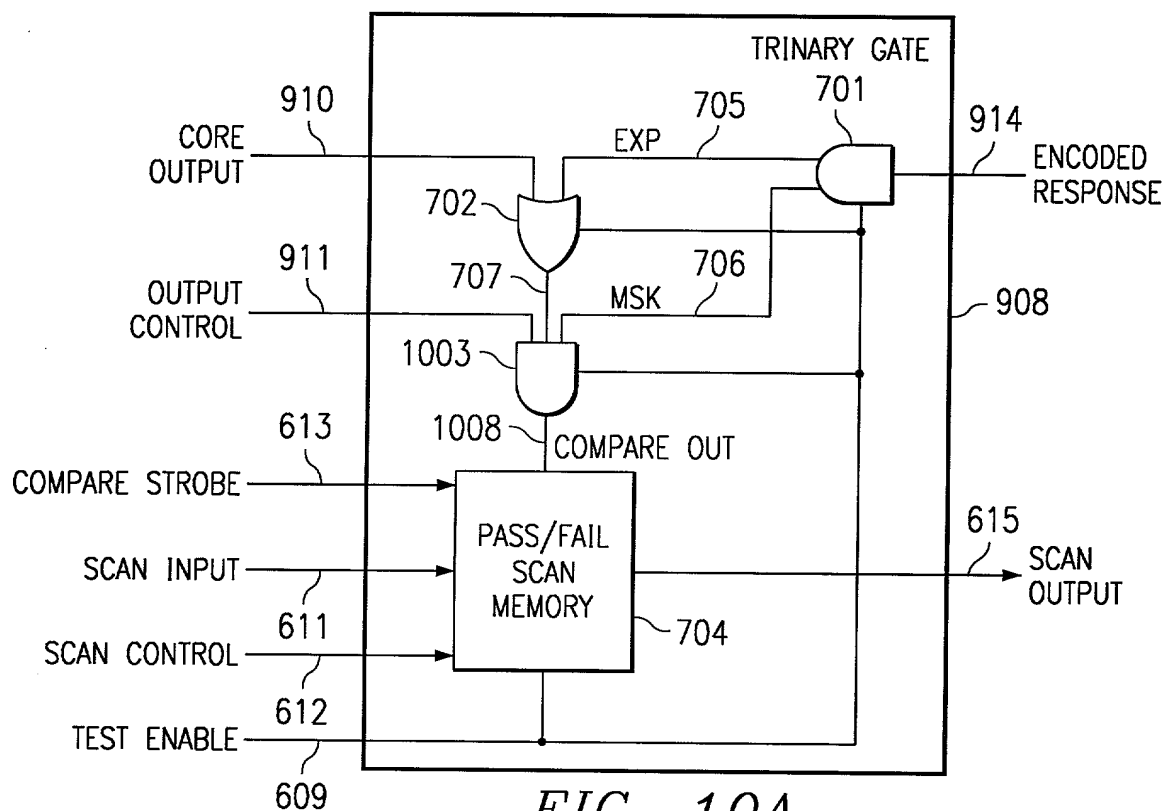


FIG. 10A

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OC	TEN	ENR	MSK	EXP	FUNCTION PERFORMED
X	0	X	X	X	TEST DISABLED
1	1	GND	1	0	COMPARE LOW
1	1	VDD	1	1	COMPARE HIGH
1	1	1/2VDD	0	X	MASK COMPARE
0	1	GND/VDD	1	0/1	TEST OUTPUT CONTROL

FIG. 10B

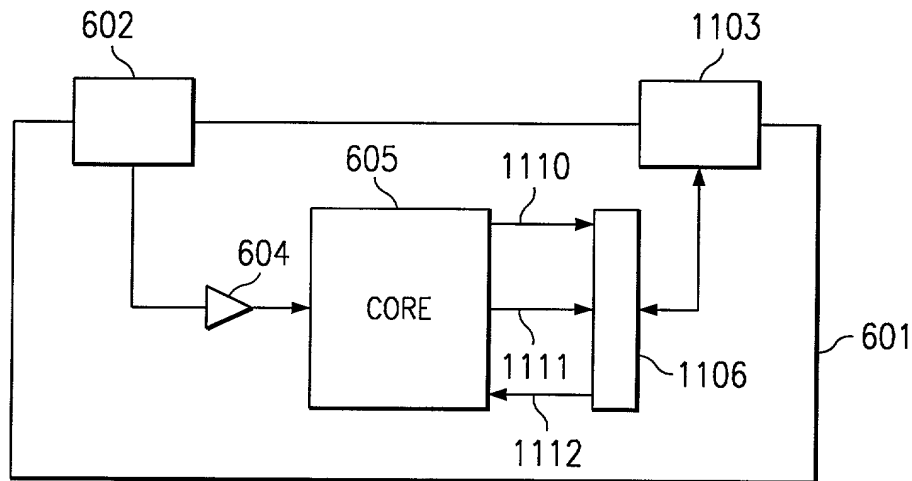


FIG. 11A

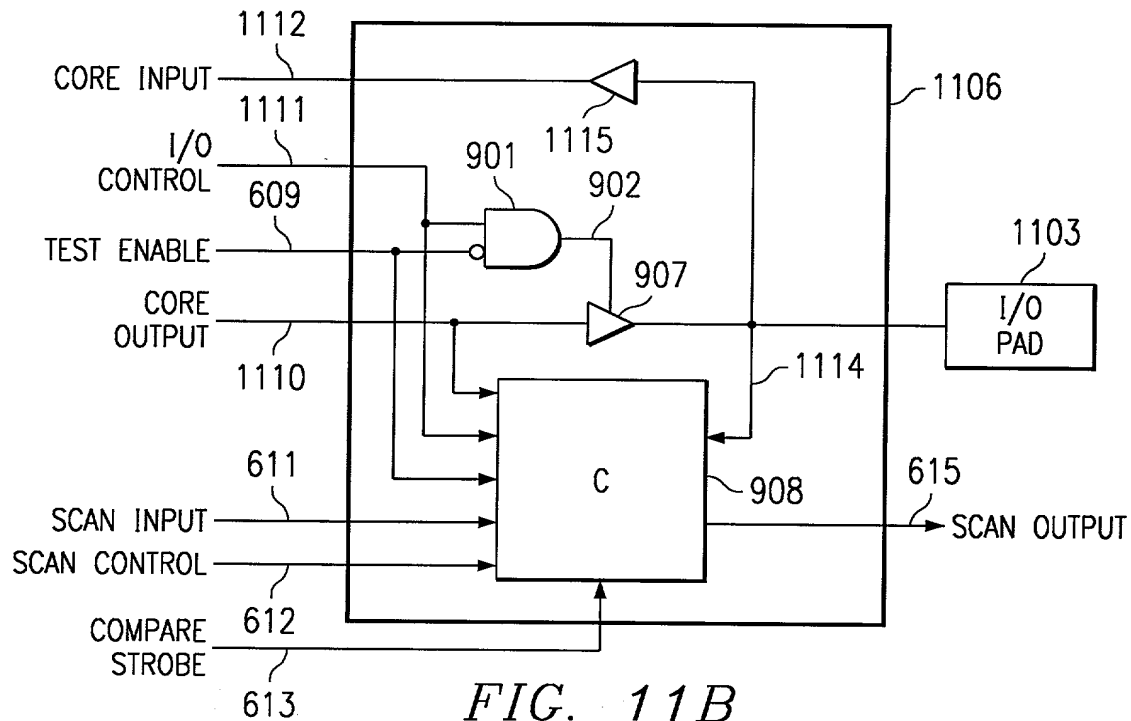


FIG. 11B

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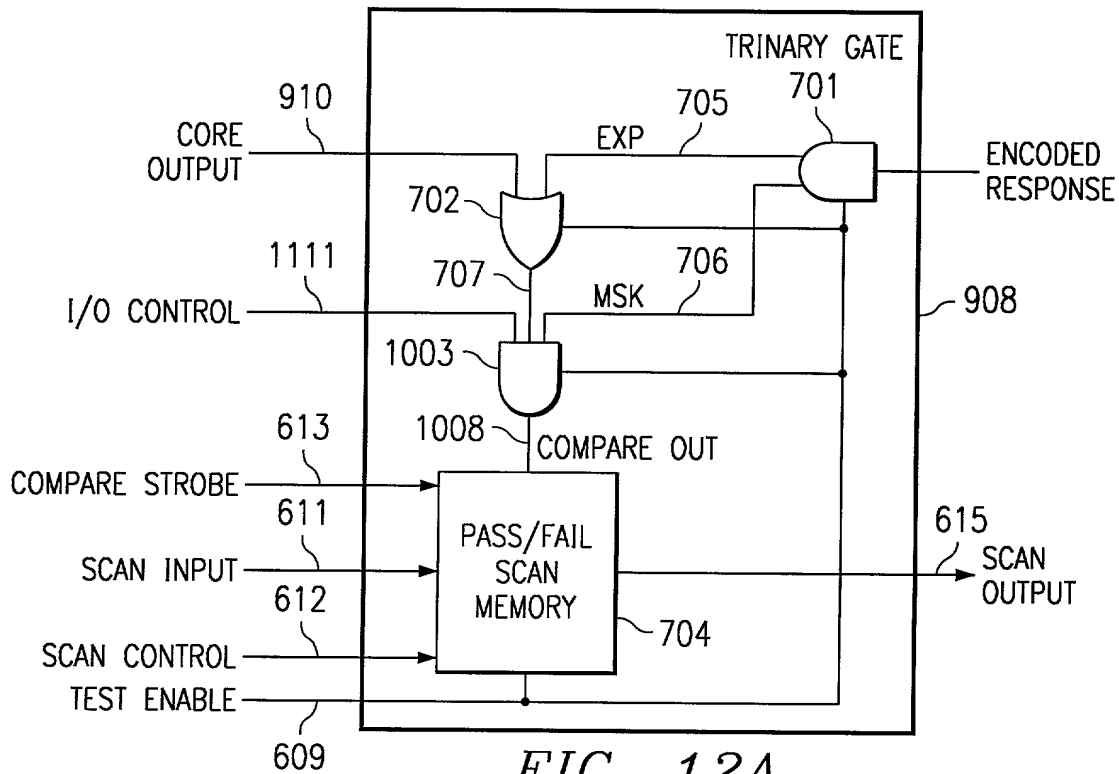


FIG. 12A

IOC	TEN	ENR	MSK	EXP	FUNCTION PERFORMED
X	0	X	X	X	TEST DISABLED
1	1	GND	1	0	COMPARE LOW
1	1	VDD	1	1	COMPARE HIGH
1	1	1/2VDD	0	X	MASK COMPARE
0	1	GND/VDD	1	0/1	TEST I/O CONTROL
0	1	GND/VDD	1	0/1	INPUT STIMULUS

FIG. 12B

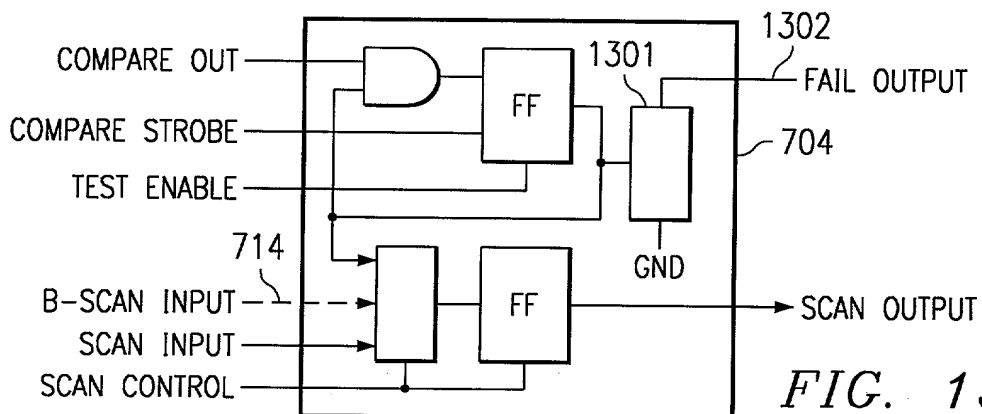


FIG. 13A

FIG. 13B

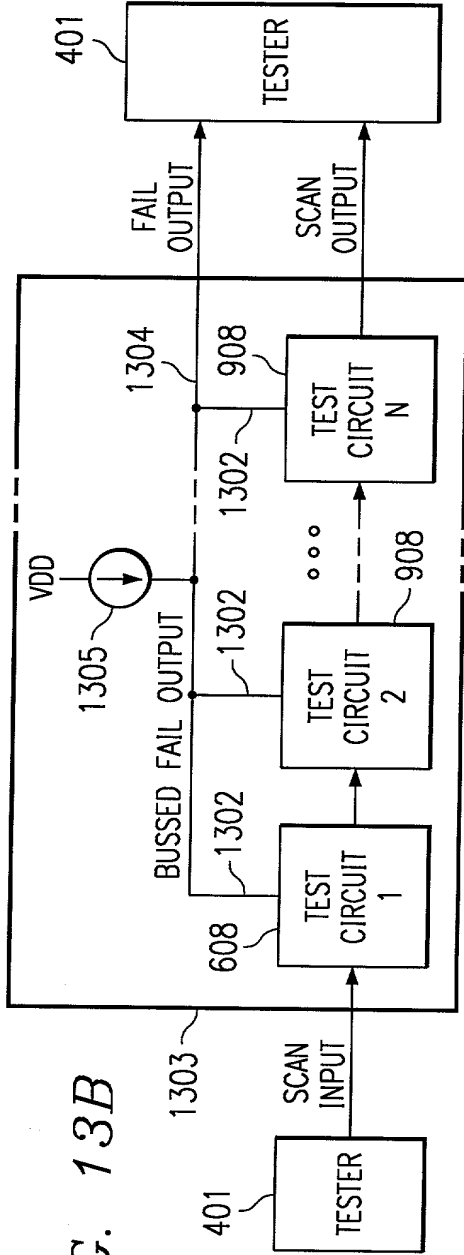


FIG. 14

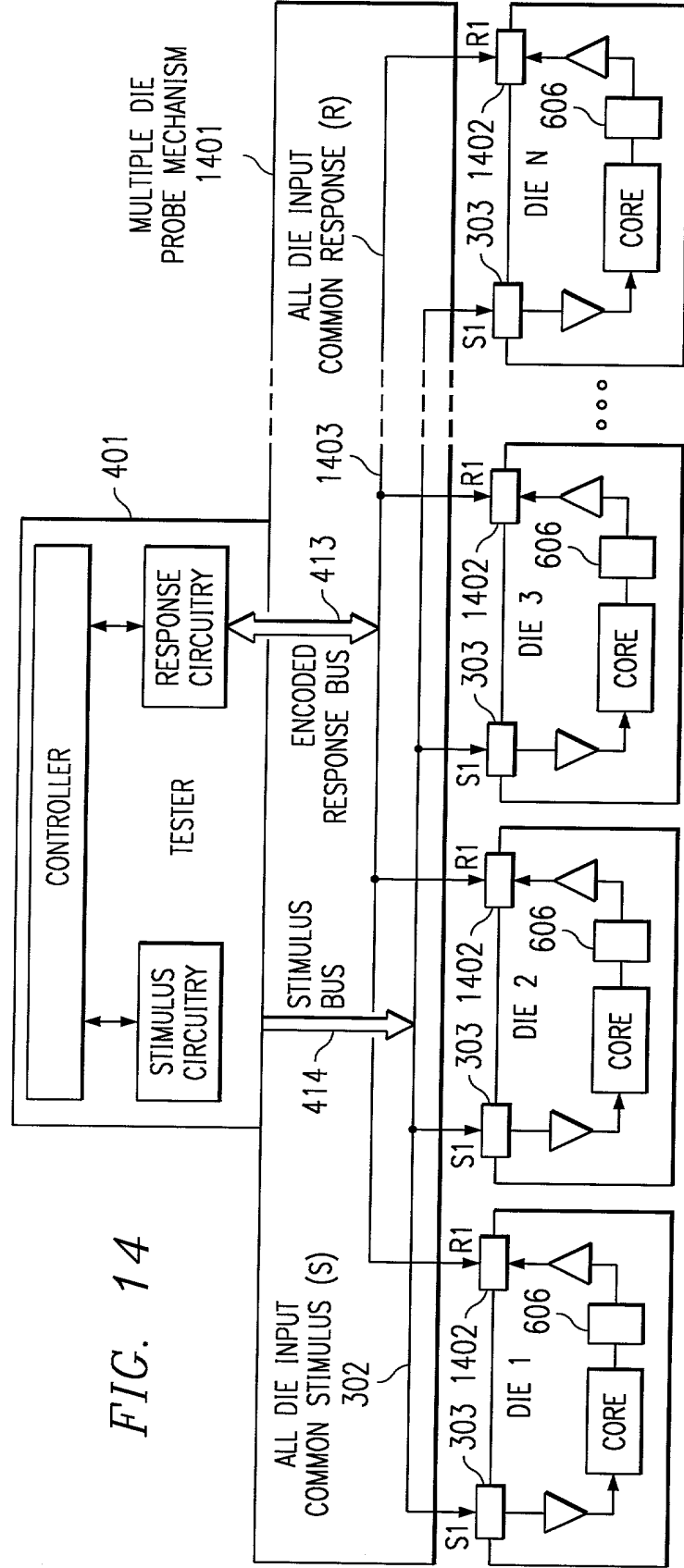
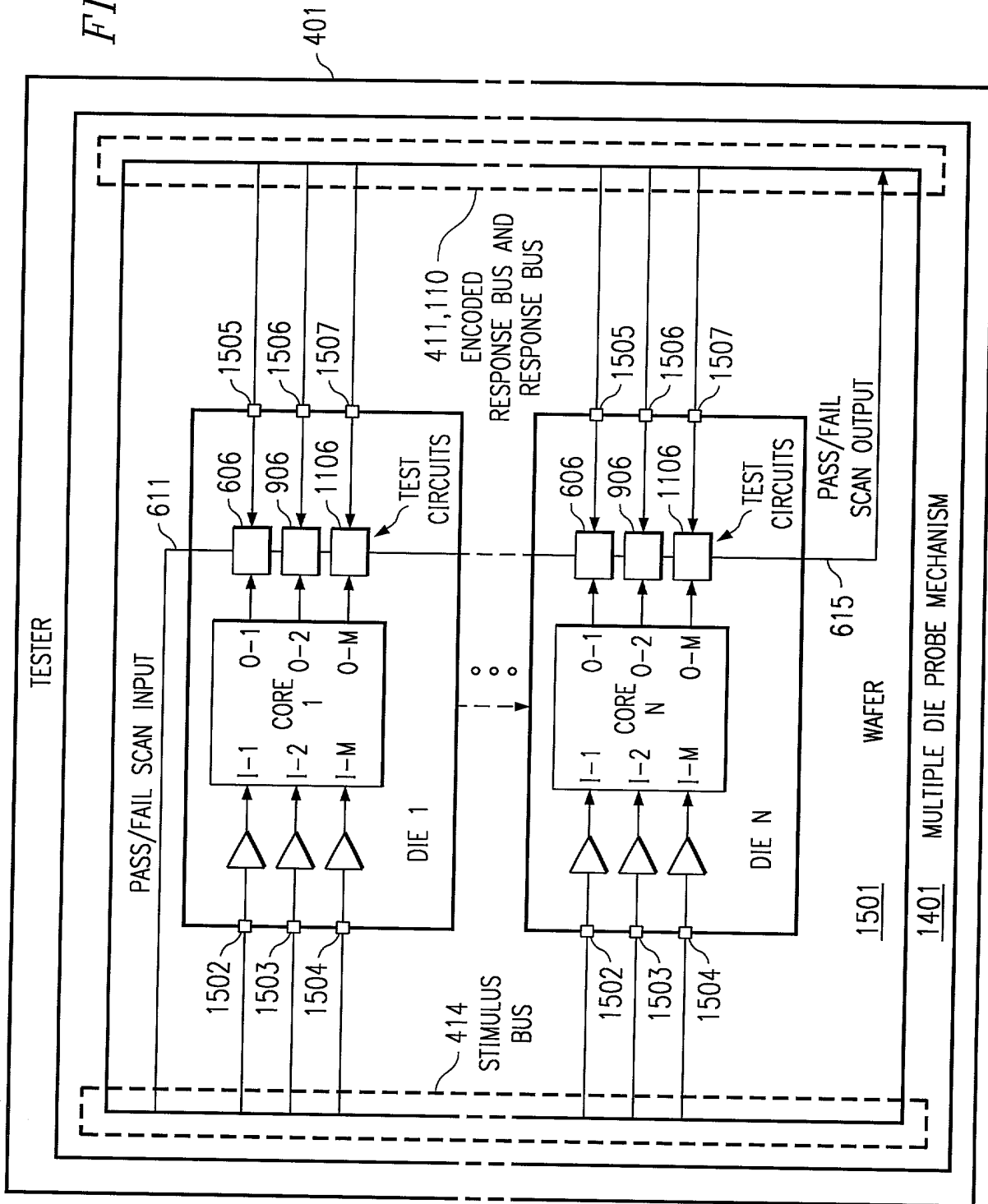


FIG. 15



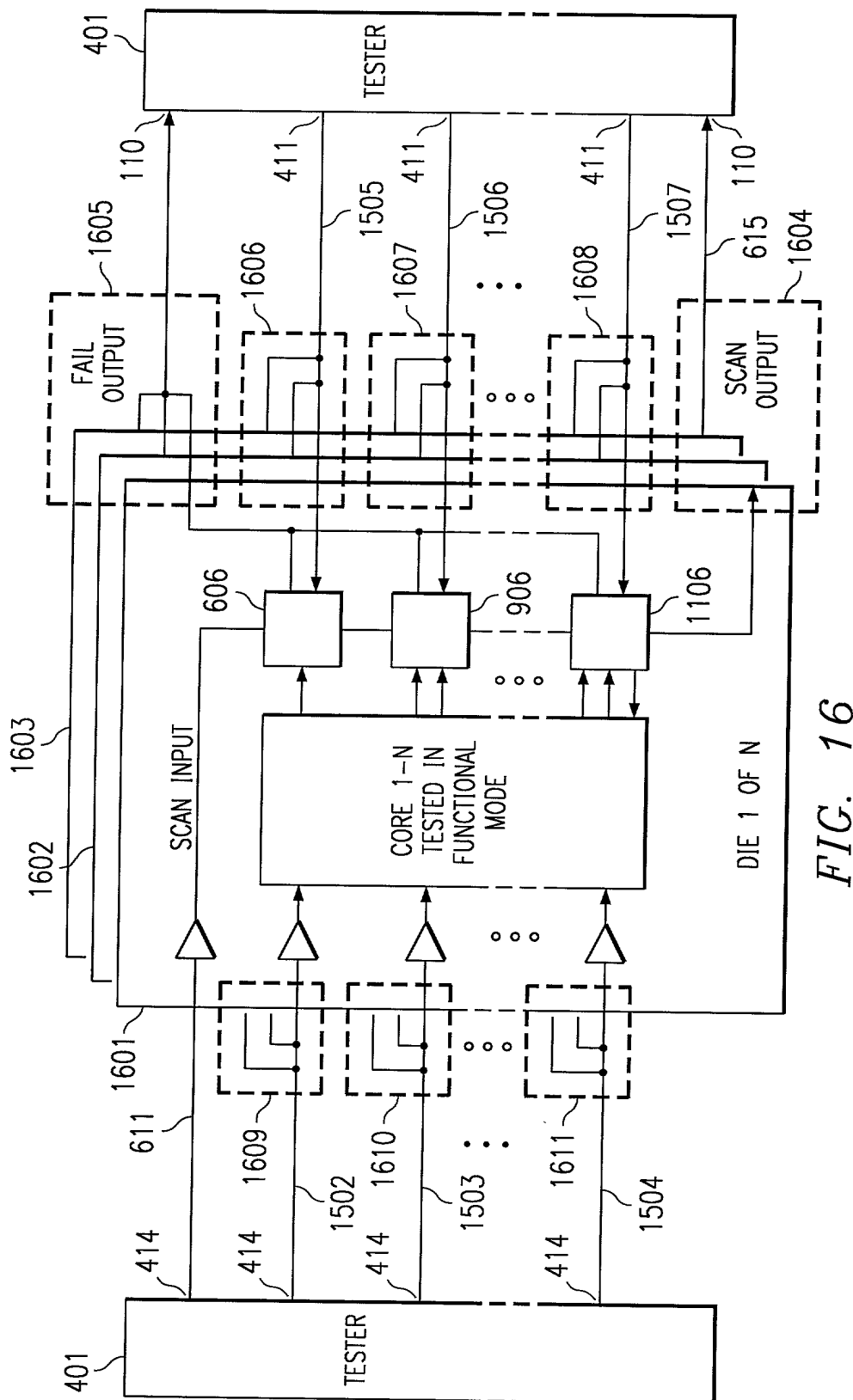


FIG. 16

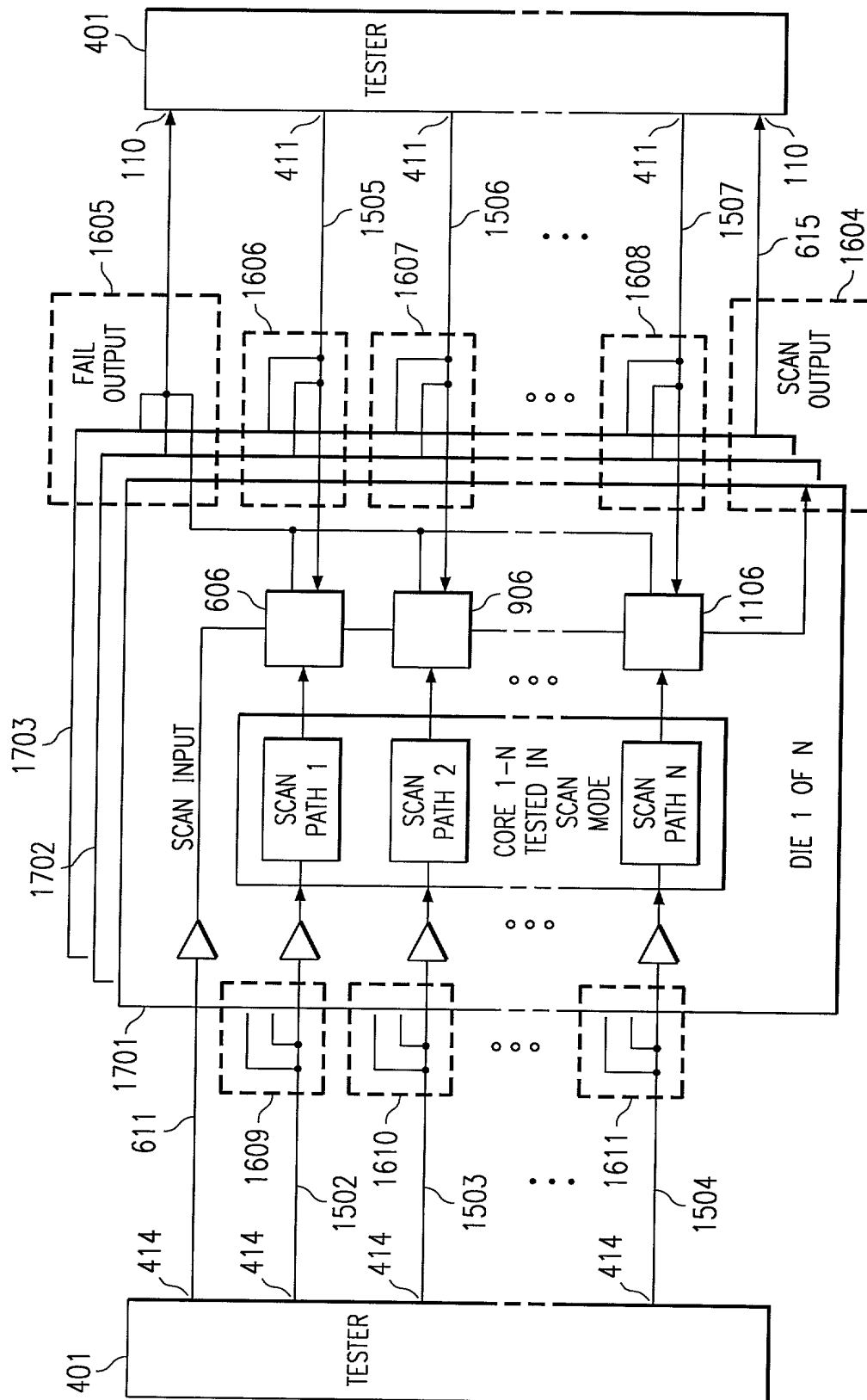


FIG. 17

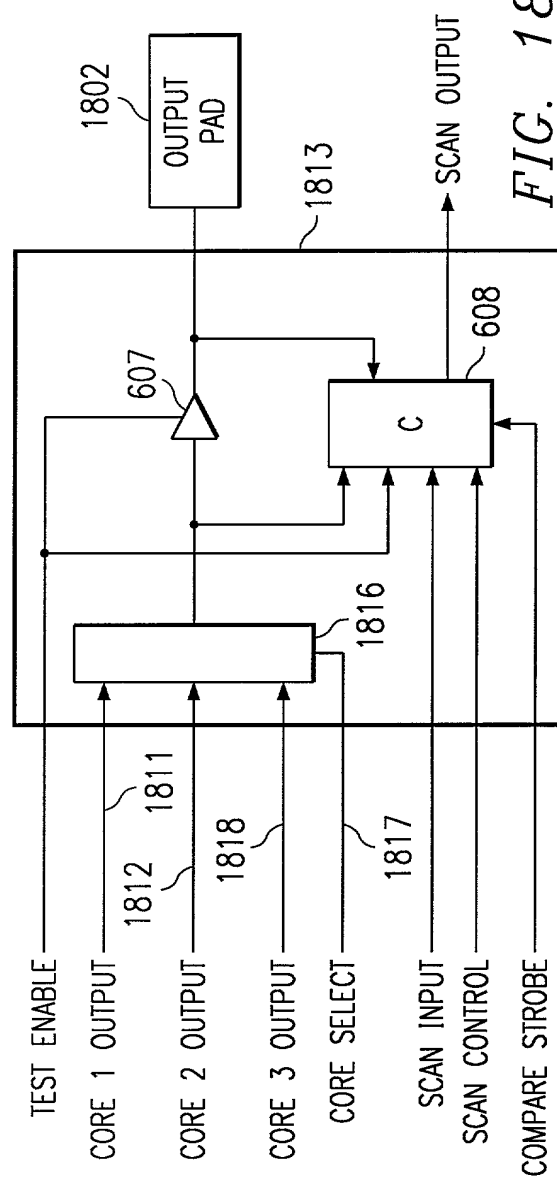
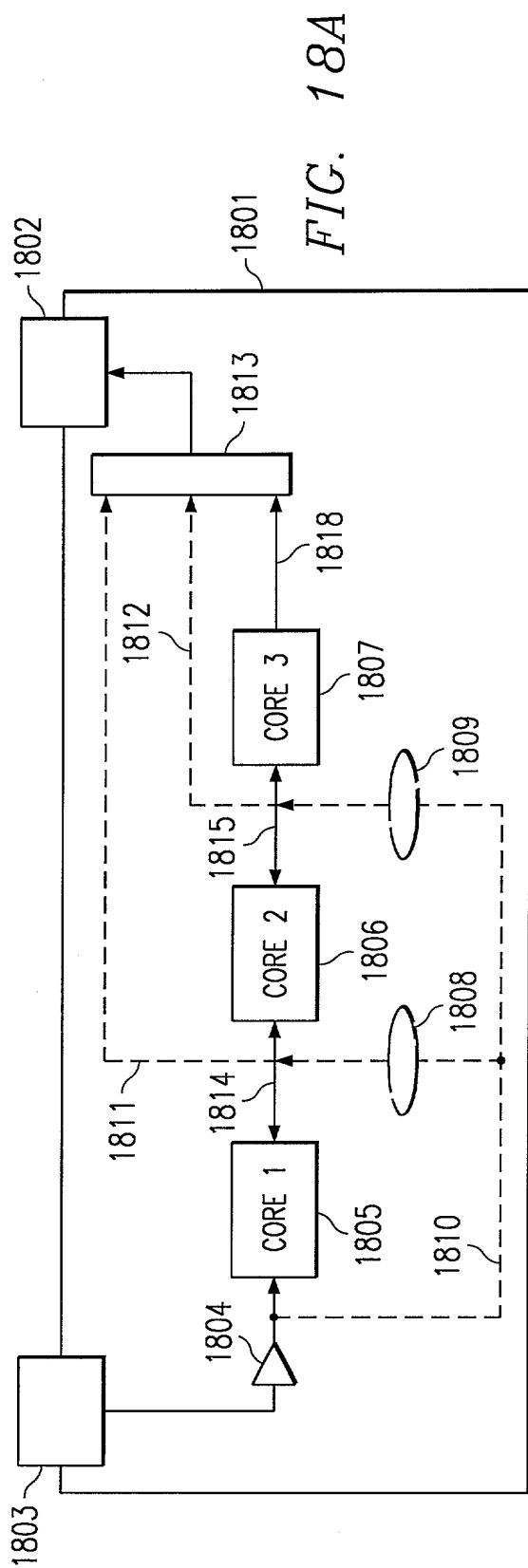
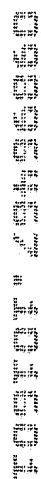


FIG. 18B

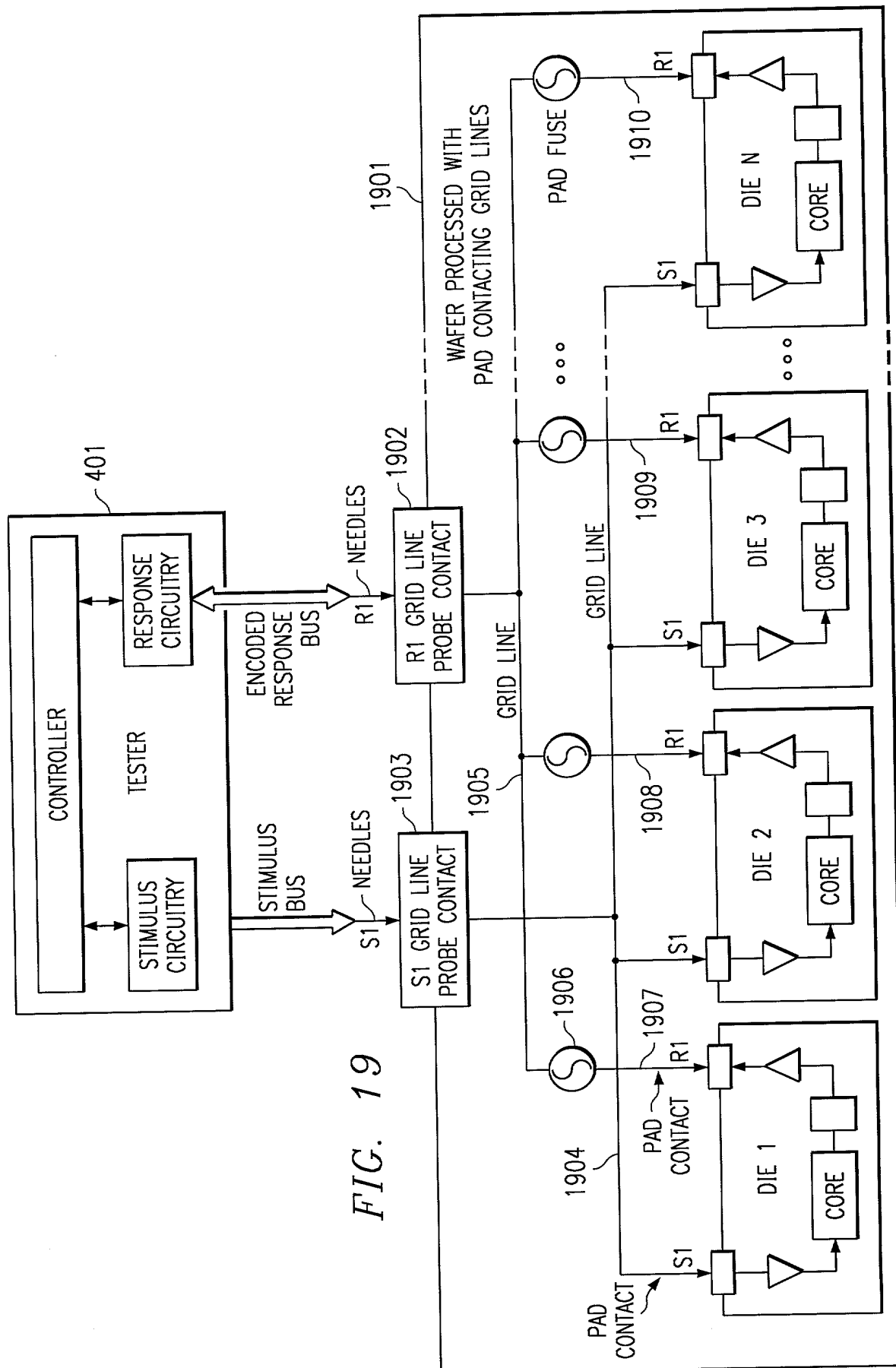
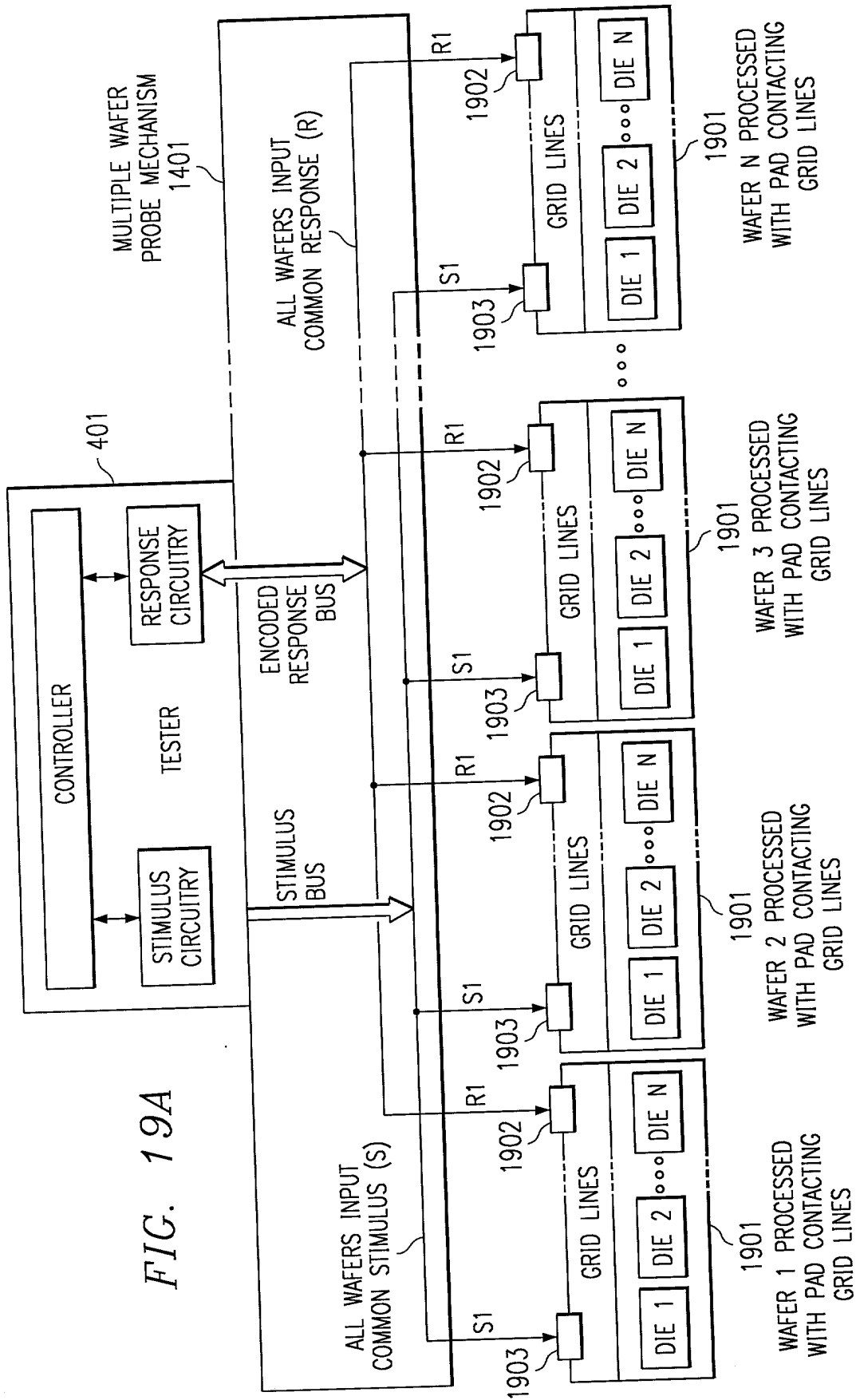


FIG. 19



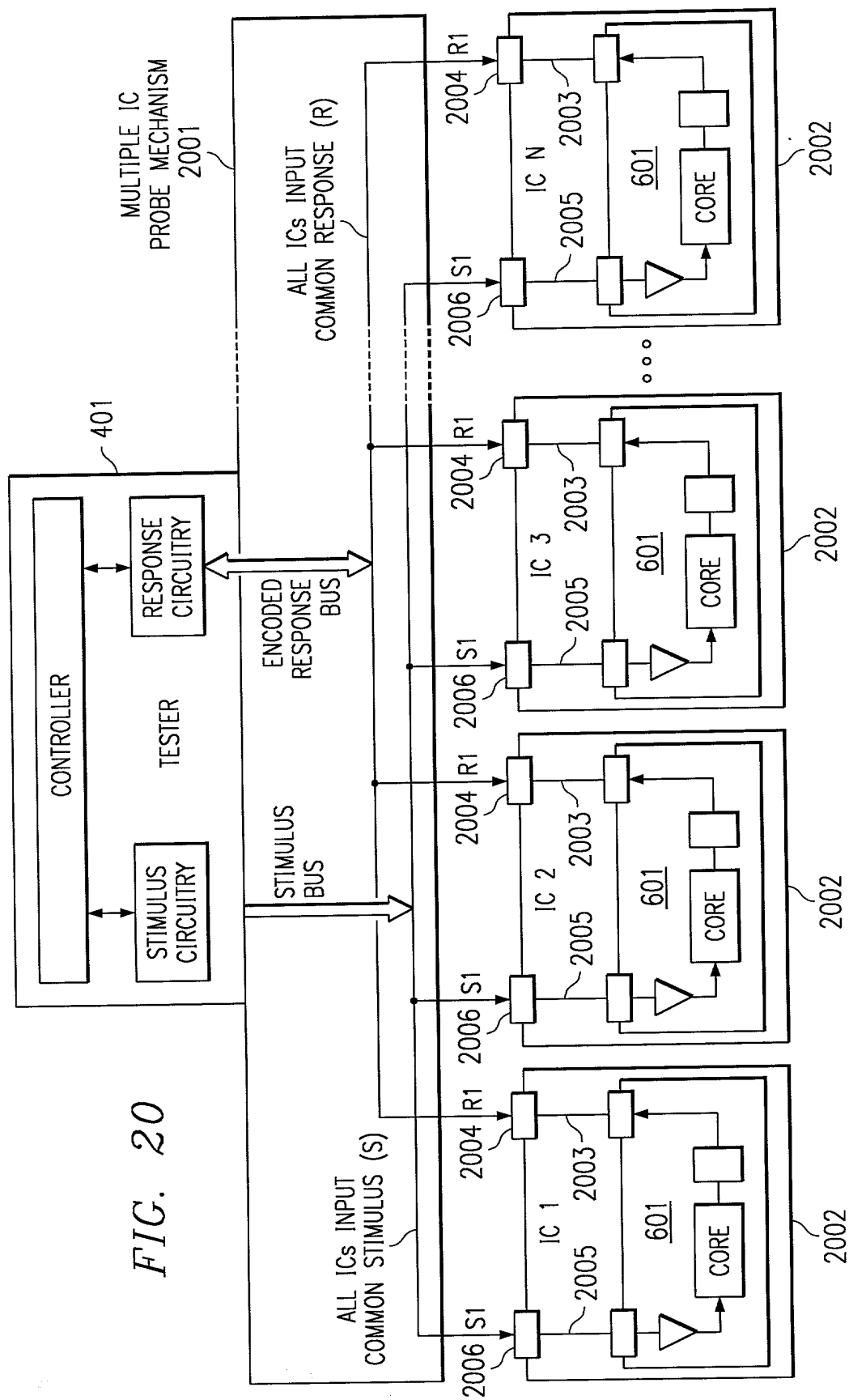


FIG. 20